What is claimed is:

1. A bus compressing apparatus comprising:

at least two bit lines, each bit line transmitting a bit signal having a voltage level;

at least two voltage control means connected to the corresponding bit lines, wherein each voltage control means changes the voltage level of the bit line at a different ratio from the other voltage control means; and

adder means for adding voltage levels outputted from the two voltage control means to generate an analog signal.

2. A bus compressing apparatus as claimed in claim 1, wherein the two voltage control means includes a first voltage control means comprising a first resistor and a second voltage control means comprising a second resistor.

3. A bus compressing apparatus as claimed in claim 2, wherein the first resistor and the second resistor have different resistance.

4. A bus compressing apparatus as claimed in claim 2, wherein the resistance value of the second resistor of the second voltage control means is $1/2^n$ of the resistance value of the first resistor, in which n is an integer.

5. A bus compressing apparatus as claimed in claim 2, wherein the resistance value of the second resistor of the second voltage control means is ½ of the resistance value of the first resistor.

6. A bus compressing apparatus as claimed in claim 2, wherein the adder means performs a wired sum operation.

7. A bus decompressing apparatus comprising:

receiving means for receiving an analog signal formed by compressing at least n-bit data, wherein n is an integer;

quantizing means for quantizing the analog signal from the receiving means; and

coding means connected to the quantizing means for coding the quantized analog signal to reconstruct the n-bit data.

8. A bus decompressing apparatus as claimed in claim 7, wherein said quantizing means includes at least (2^n-1) level detectors connected in parallel between the receiving means and the coding means, each level detector being configured to detect different voltage levels of the analog signal.

9. A bus decompressing apparatus as claimed in claim 8, wherein each one of the level detectors comprises:

a transistor controlled by the analog signal from the receiving means; and

output voltage control means connected to the transistor to output the quantized analog signal to the coding means in response to the analog signal.

10. A bus decompressing apparatus as claimed in claim 9, wherein the output voltage control means includes a pull-up resistor.

11. A bus decompressing apparatus as claimed in claim 9, wherein the transistor is an NMOS transistor having a threshold voltage which turns on when the analog signal is above the threshold voltage and turns off when the analog signal is below the threshold voltage.

12. A bus decompressing apparatus as claimed in claim 11, wherein the transistor is connected between a source voltage and a ground and the threshold voltage of the transistor for each level detector is different by a voltage value approximately equal to the source voltage divided by the number of level detector in the bus decompressing apparatus.

13. A bus decompressing apparatus as claimed in claim 8, the quantizing means includes first, second and third level detectors, each level detector having a transistor with a threshold voltage, the transistor being connected between a first voltage and a second voltage, wherein the transistor of the first level detector turns on when the analog signal is above the second voltage, the transistor of the second level detector turns on when the analog signal is above the second voltage by about 1/3 of the difference between the first and second voltages, and the transistor of the third level detector turns on when the analog signal is above the second voltage by about 2/3 of the difference between the first and second voltages.

14. A bus decompressing apparatus as claimed in claim 7, wherein the coding means transforms the quantized analog signal to n-bit digital signals.

15. A bus decompressing apparatus as claimed in claim 13, the coding means receives an output of the second level detector to generate an n-th bit data.

16. A data interfacing apparatus comprising:

bus compressing means for compressing at least two bit data into an analog signal; and

bus decompressing means installed in a data terminal for decompressing the analog signal from the data compressing means into the at least two bit data.

17. A liquid crystal display comprising:

a liquid crystal panel;

driver integrated circuits for selectively driving the liquid crystal panel with at least two bit data;

signal input means for inputting an analog signal representing at least two bit data being compressed to form the analog signal; and

bus decompressing means connected to the signal input means for decompressing the analog signal to generate two bit data and for supplying the decompressed two bit data to the driver integrated circuits.

18. A liquid crystal display as claimed in claim 17, wherein the bus decompressing means is positioned within each one of the driver integrated circuits, and the signal input means is connected to the driver integrated circuits.

19. A liquid crystal display as claimed in claim 17, the bus decompressing means includes level detectors, inputs of which are connected to the analog signal and outputs are connected to a coding device, wherein each level detector is configured to detect different voltage levels of the analog signal.

20. A liquid crystal display as claimed in claim 19, wherein each one of the level detectors comprises:

a transistor controlled by the analog signal; and

output voltage controller connected to the transistor to output the quantized analog signal to the coding device in response to the analog signal.

21. A liquid crystal display as claimed in claim 20, wherein the output voltage controller includes a pull-up resistor.

22. A liquid crystal display as claimed in claim 20, wherein the transistor is an NMOS transistor having a threshold voltage which turns on when the analog signal is above the threshold voltage and turns off when the analog signal is below the threshold voltage.

23. A liquid crystal display as claimed in claim 22, wherein the transistor is connected between a source voltage and a ground and the threshold voltage of the transistor for each level detector is different by a voltage value approximately equal to the source voltage divided by the number of level detector in the bus decompressing apparatus.

24. A liquid crystal display as claimed in claim 17, the decompressing means includes first, second and third level detectors, each level detector having a transistor with a threshold voltage, the transistor being connected between a first voltage and a second voltage, wherein the transistor of the first level detector turns on when the analog signal is above the second voltage, the transistor of the second level detector turns on when the analog signal is above the second voltage by about 1/3 of the difference between the first and second voltages, and the transistor of the third level detector turns on when the analog signal is above the second voltage by about 2/3 of the difference between the first and second voltages.

25. A bus compressing apparatus for use in interfacing a controller and a display device for compressing n output signals of the controller, the bus compressing apparatus comprising:

n voltage converters coupled to the corresponding output signals, wherein n is an integer and each voltage converter changes a voltage level of the corresponding output signal, and outputs of the n voltage converters are

connected to produce a combined output signal in response to voltage levels of the n output signals from the controller, and wherein the combined output signal has a plurality of voltage levels representing nth power of the number of output signals.

26. A bus compressing apparatus of claim 25, wherein each one of the n voltage converters includes a resistor.

27. A bus compressing apparatus of claim 26, wherein each resistor in corresponding n voltage converters has a different resistance.

28. A bus compressing apparatus of claim 26, wherein the resistance value of each resistor of the n voltage converters is $1/2^n$ of the resistance value of the resistor for a first voltage converter.

29. A bus decompressing apparatus comprising:

an input line transmitting an analog signal formed by compressing n-bit data, wherein n is an integer;

a plurality of level detectors parallely connected to the input line to output a quantized signal; and

a coding device connected to the plurality of level detectors to code the quantized signal to reconstruct the n-bit data.

30. A bus decompressing apparatus of claim 29, wherein the plurality of level detectors includes at least (2^n-1) level detectors, each level detector being configured to detect different voltage levels of the analog signal.

31. A bus decompressing apparatus of claim 30, wherein each one of the level detectors comprises:

a transistor controlled by the analog signal from the receiving means; and

a resistor connected to the transistor to output the quantized signal to the coding device in response to the analog signal.

32. A bus decompressing apparatus of claim 31, wherein the transistor is an NMOS transistor having a threshold voltage which turns on when the analog signal is above the threshold voltage and turns off when the analog signal is below the threshold voltage.

33. A bus decompressing apparatus of claim 32, wherein the transistor is connected between a source voltage and a ground and the threshold voltage of the transistor for each level detector is different by a voltage value approximately equal to the source voltage divided by the number of level detector in the bus decompressing apparatus.